REMARKS

In the Office Action, originally numbered Claims 1-28 were examined and are rejected. In response to the Office Action, Claims 6, 8-11, 21 and 28 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-28 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §112

The Examiner has rejected Claim 6 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Applicants regard as the invention. Applicants respectfully traverse this rejection.

In response, Applicants have amended the preamble of Claim 6, such that Claim 6, as amended, now particularly points out and distinctly claims the subject matter, which Applicants regard as the invention. Therefore, in view of Applicants' amendment to Claim 6, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, second paragraph, rejection of Claim 6.

The Examiner has rejected Claim 28 (original Claim 29) for reciting the limitation "the SDRAM" in line 1, as there is insufficient antecedent basis for this limitation in the claim. In addition, the Examiner has indicated that the numbering of the claims is not in accordance with 37 C.F.R.§1.126, which requires the original number of the claims to be preserved throughout the prosecution.

Applicants note that there was no Claim 27 submitted with the filed patent application. In accordance with the Examiner's request, misnumbered Claims 28 and 29 have been renumbered to Claims 27 and 28. In addition, Applicants have amended Claim 28 to depend from Claim 27 to overcome the antecedent basis issue. Therefore, Applicants request withdrawal of the rejection of Claim 28.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1-28 (original filed Claims 1-26, 28 and 29, there is no Claim 27) under 35 U.S.C. §103(a) as being unpatentable over G.B. Patent No. 2,386,442 to

Lewis ("Lewis") in view of U.S. Patent No. 6,477,177 issued to Potts ("Potts"). Applicants respectfully traverse this rejection.

Regarding Claims 1 and 6, Claims 1 and 6 recite the following claim features, which are neither disclosed nor suggested by Potts:

> enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element; and
>
> granting the processing element ownership over the selected hardware accelerator. (Emphasis added.)

The Examiner has cited the combination of Lewis in view of Potts to render the above-recited features of Claims 1 and 6 obvious. For at least the reasons described below, Applicants respectfully submit that the combination of Lewis in view of Potts fails to either teach or suggest each of the above-recited features of Claims 1 and 6. Furthermore, one skilled in the art would not combine the teachings of Lewis in view of Potts as suggested by the Examiner.

In contrast to the above-recited features of Claims 1 and 6, Lewis discloses:

> a data processing system for allocation of data into timeframes and allocation of particular timeframe data to a particular processor for use in mobile communication terminals such as a mobile phone where data is received in air interface timeslots. (*See*, Abstract.) (Emphasis added.)

As shown in FIG. 1 of Lewis, the schematic processor arrangement 10 illustrates a controller 12, which oversees distribution of data throughout the processor, as well as DSP1 and DSP2. (*See*, pg. 4, lines 3-5.) As further shown in FIG. 1 of Lewis, reconfigurable logic blocks (11A, 11B, 11C) may be hardware accelerators or a reconfigurable portion of a hardware accelerator and are preferably fully shared and hence, available for use by all DSPs in the multi-processor system. (*See*, pg. 4, lines 9-18 of Lewis.) As further disclosed by Lewis:

> When performing a given function, the DSPs may require the use of one or more of the RLBs in order to accelerate the operation. In accordance with a first embodiment of the present invention, the assignment of data to the plurality of digital signal processors in the multi-processor system is based upon a timeslot/frame structure. One or more sets of data are allocated to a single frame or timeslot and all processing for a given timeslot is undertaken by an individual DSP. Each processor can be configured to perform a number of sequential tasks, which reduces the need to move large amounts of data between processors. (pg. 4, lines 20-27.) (Emphasis added.)

Accordingly, based on the cited passage above, the DSPs, disclosed by Lewis operate based on a timeslot/frame structure when data is received. As further described by Lewis:

> Another embodiment of the invention is directed to the efficient allocation of RLB resources, particularly with a view to overcoming the time normally taken to reconfigure RLBs and ensuring that a block is available to a processor when required. In this regard, each RLB may be marked so as to indicate its current configuration as well as with an indication of the status of the block such as whether it is free or busy. These indications may be provided, for example, by various storage means, such as via flags associated with the blocks or via updateable look-up tables or lists. (pg. 5, lines 26-32.) (Emphasis added.)

To enable the efficient allocation of RLB resources, Lewis teaches that a controller is responsible for systematic allocation of RLB resources. Specifically, as disclosed by Lewis:

> In operation, the controller would be notified that a DSP wants a particular function. The controller would then check all free blocks to determine if that function is already configured in a free block. If so, then the DSP is allocated the pre-configured block. Alternatively, if no free block is appropriately configured, then any free block is reconfigured and allocated to the DSP. In this way, reconfigurable blocks are more likely to be available when required and without the need for reconfiguration. (pg. 6, lines 6-11.) (Emphasis added.)

As further disclosed by Lewis:

> In another embodiment of the invention, the controller decides which block to assign to each DSP based upon knowledge of reconfiguration time and current thread of each device. For example, where four DSPs exist in the multi-processor system, the controller could keep a list, in a storage means, of all the configuration functions required by the respective DSPs during the first cycle of timeslots for the four DSPs. This list could be updateable after each processor completes processing the one or more sets of data associated with its designated timeslot. (pg. 6, lines 25-31.) (Emphasis added.)

Accordingly, based on the cited passages above, controller 12, as disclosed by Lewis, is responsible for the allocation of RLBs between DSPs 1 and 2, which may require the controller to keep a list of configuration functions required by DSPs to perform the desired allocation once notified that a particular DSP desires a particular function. (*See*, supra.)

Accordingly, based on the cited passages above, Applicants respectfully submit that DSPs 1 and 2, as taught by Lewis, do not select a desired RLB (11A-11C). As disclosed by Lewis, such operation is performed by the controller when notified that a particular DSP wants a particular function/resource. In further embodiments disclosed by Lewis, the controller decides

which block to assign to each DSP based on knowledge of reconfiguration time and the current thread of each device. (*See*, pg. 6, lines 25-27.) Accordingly, rather than allowing DSPs to select a desired RLB (11A-11C), such functionality is taken away from DSPs and is performed by controller 12, as taught by Lewis, to achieve the goal of overcoming the time normally taken to reconfigure RLBs and ensuring that a block is available to a processor when required. (*See*, pg. 5, lines 26-32.)

Conversely, as recited by Claims 1 and 6, a processing element selects a hardware accelerator by setting a bit of a register within a register file, which causes enablement of the selected hardware accelerator and the grant of ownership to the processing element over the selected hardware accelerator. Accordingly, Lewis fails to teach or suggest the above-recited features of Claims 1 and 6 by assigning the efficient allocation of RLB resources to controller 12; hence, DSP1 and DSP2 do not select an RCLB (11A-11C), an RCLB is assigned by controller 120. (*See*, pg. 6, lines 5-11 and 25-31.)

To rectify the deficiencies of Lewis, the Examiner cites Potts. In contrast to the above-recited features of Claims 1 and 6, Potts discloses:

> Conventional AC '97 split-architecture systems accommodate only one processor, treating the AC '97 link as a single device to be used by only one processor. However, it has been appreciated by the present inventor that more recent applications would benefit from access to the AC '97 link and the AC '97 Analog sub-system by a plurality of processors, either all within the AC controller sub-system 500 and/or external to the AC controller sub-system 500. There is thus a need for an interface in an AC controller system which can provide access to the AC '97 link and AC '97 Analog sub-system by any of a plurality of processors. (col. 3, lines 1-11.) (Emphasis added.)

Applicants respect fully submit that the disclosure in Potts is limited to enabling an AC'97 split-architecture system to accommodate more than one processor. (*See*, supra.) The use of an AC '97 split-architecture system to accommodate more than one processor provides no teachings nor suggestions regarding the capability to share a plurality of hardware accelerators among a plurality of processing elements of a media signal processor to enable a processing element to gain ownership over a selected hardware accelerator, as recited by Claims 1 and 6.

Potts describes the above functionality as follows:

> In accordance with the principles of the present invention, access is provided to an AC '97 link or other digital serial interface by any of a plurality of

processing agents with an arbitration scheme which is provided on a per channel basis, either during power up of the AC '97 devices or as the accesses occur. Thus, e.g., each channel or time slot in an AC '97 link can be considered to be an independent resource which is configurable for access by any of a plurality of requesting processors. (col. 4, lines 49-58.) (Emphasis added.)

Accordingly, based on the cited passages of Potts, each channel or timeslot in an AC link can be considered as an independent resource, which is configurable for access by any of a plurality of requesting processors. (*See*, col. 4, lines 55-58.) Applicants respectfully submit that the capability to provide each channel or timeslot within an AC link as an independent resource inevitably results in the sharing of the AC link between each of the processors, as disclosed in Potts. (*See*, supra.) Hence, Applicants respectfully submit that the disclosure in Potts is expressly limited to time sharing of a single resource.

As mandated by case law, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Here, Lewis explicitly teaches that controller 10 is responsible for the systematic allocation of free RLBs, as well as the assignment of an RLB when a DSP requires a particular function/resource. (*See*, pg. 6, lines 6-11 and 25-31 of Lewis.) According to the Examiner, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the register file of Potts into the system of Lewis to allow the plurality of processing elements to better and more efficiently share access to one of the plurality of resources (such as hardware accelerators or timeslot registers), as taught by Potts (col. 6, lines 37-45). (*See*, pg. 3, ¶2 of the Office Action mailed December 20, 2005.)

As shown in FIGS. 1 and 2 of Potts, packer/unpacker unit (PUP) digital interface 110 incorporates the various data written by processors 120 and 122 to timeslot registers (210, 211, 212, . . . 220). The data from these various timeslot registers 210-222 is combined into a 256 bit stream, which is provided to AC link via output FIFO 240. Hence, the disclosure in Potts is simply limited to use of configuration control registers to allow processors 120 and 122 to gain access to a desired timeslot register.

Accordingly, assuming one skilled in the art were to modify Lewis in view of Potts, the combination of Lewis in view of Potts would simply be limited to providing DSPs with the

capability to request a desired RLB. However, as disclosed by Lewis, it is the responsibility of the controller to perform the assignment of RLBs. Consequently, modification of Lewis in view of Potts would merely provide a means for notifying controller 12 that a DSP requires an RLB or a particular function provided by an RLB.

As disclosed by Lewis in response to notification that a DSP requires a resource/function, the controller decides which block to assign each DSP, for example, based on knowledge of reconfiguration time and the current thread of the device, which could be performed by the controller maintaining a list of configuration functions required by respective DSPs. (*See*, pg. 6, lines 25-31.) Hence, the combination of Lewis in view of Potts fails to disclose the enablement of a hardware accelerator selected according to a bit within a register file set by a processing element and the granting of such processing element with ownership over the selected hardware accelerator, as recited by Claims 1 and 6.

Consequently, Applicants respectfully submit that the combination of Lewis in view of Potts fails to teach or suggest each of the recited features of Claims 1 and 6, as required to establish a *prima facie* case of anticipation. In re Royka, supra.

Furthermore, Applicants respectfully submit that Potts teaches away from the modification of Potts suggested by the Examiner to include the functionality of the packer/unpacker (PUP) digital interface module 110, which is controlled by control register 220 to control access by a plurality of register resources in the PUP 200, such as timeslot registers 210-222. As required by case law:

> It is improper to combine references where the references teach away from their combination. In re Grasselli, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983).

As indicated above, an objective of Lewis is the efficient allocation of RLB resources, particularly with a view to overcoming the time normally taken to reconfigure RLBs and ensuring that a block is available to a processor when required. (*See*, pg. 5, lines 26-28.) To achieve such functionality, Lewis teaches a controller to provide a systematic allocation of free RLBs. Applicants respectfully submit that providing such functionality within controller 12 is required by Lewis since:

> The assignment of data to the plurality of digital signal processors in the multi-processor system is based upon a timeslot/frame structure. (pg. 4, lines 22-23.)

Accordingly, as disclosed by Lewis, data is allocated to a signal frame or timeslot and all processing for a given timeslot is undertaken by an individual DSP such that processors can be configured to perform a number of sequential tasks, which reduces the need to move large amounts of data between processors. (*See*, pg. 4, lines 23-27.) The timeslot/frame structure for assignment of operation of the various DSPs is required by Lewis since the multi-processing system in Lewis is designed for use in mobile communication terminals, such as a mobile phone where data is received in error interface timeslots. (*See*, Abstract of Lewis.)

Applicants respectfully submit that one skilled in the art would not be motivated to modify Lewis as disclosed by Potts, as suggested by the Examiner. Specifically, allowing a DSPs to select their specifically desired RLB would require additional knowledge and functionality within the DSPs to achieve the objective of efficient allocation of RLB resources, particularly with a view to overcoming the time normally taken to reconfigure RLBs and ensuring that a block is available to a processor when required. (*See*, pg. 5, lines 26-32.)

Therefore, Applicants respectfully submit that Lewis teaches away from the inclusion of combining the register file of Potts with the system of Lewis to allow the processor to perform the allocation of RLBs 210-220, since one skilled in the art would recognize that such functionality is performed by the controller taught by Lewis. Hence, Lewis teaches away from allowing DSPs 1 and 2 performing allocation of RLBs 210-222. Consequently, Applicants respectfully submit that the Examiner is prohibited from combining the teachings of Lewis and Potts since Lewis teaches away from the combination. Id.

Moreover, Applicants respectfully submit that the modification of Lewis in view of Potts, as suggested by the Examiner, would render Lewis and Potts unsatisfactory for their intended purpose of efficient allocation of RLB resources. (*See*, Lewis, pg. 5, lines 26-28.) As established by case law:

> If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed.Cir. 1984).

Applicants respectfully submit that the inclusion of control register 220 and timeslot registers 210-222 of PUP 200 within Lewis could render Lewis unsatisfactory for its intended purpose of the efficient allocation of RLB resources with a view to overcoming the time required to reconfigure RLBs to ensure that a block is available to a processor when it is required. (*See*, pg. 5, lines 26-28 of Lewis.)

Accordingly, Applicants respectfully submit that one skilled in the art would not modify Lewis in view of Potts, as suggested by the Examiner, since such modification would render Lewis unsatisfactory for its intended purpose. Therefore, a suggestion or motivation for the modification suggested by the Examiner is lacking and therefore the Examiner fails to provide a *prima facie* case of obviousness of Claims 1 and 6. Id.

Therefore, Applicants respectfully submit that Claims 1 and 6 are patentable over the combination of Lewis in view of Potts. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1 and 6.

Regarding Claims 2-5 and 7-10, Claims 2-5 and 7-10, based on their dependency from Claims 1 and 6, respectively, are also patentable over the combination of Lewis in view of Potts. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 2-5 and 7-10.

Regarding Claims 11 and 21, Claims 11 and 21 recite the following claim feature, which is neither taught nor suggested by the combination of Lewis in view of Potts:

> a register file coupled to the selection unit and the plurality of processing elements, the register file including a plurality of general purpose registers accessible by the plurality of hardware accelerators, the selection unit and the plurality of processing elements, at least one of the general purpose registers including at least one bit to allow a processing element to select a hardware accelerator; and
>
> a control unit to direct the selection unit to activate the selected hardware accelerator to grant the processing element ownership over the selected hardware accelerator. (Emphasis added.)

Applicants respectfully submit that the above-recited features of amended Claims 11 and 21 are analogous to the above-recited features of Claims 1 and 6. Consequently, Applicants' arguments provided above with regard to the §103(a) rejection of Claims 1 and 6 as obvious over the combination of Lewis in view of Potts equally apply to the Examiner's §103(a) rejection of Claims 11 and 21.

Applicants respectfully submit that Potts fails to disclose a register file, as recited by amended Claims 11 and 21. As disclosed by Potts, the capability to write to a timeslot requires the processor to write to a configuration control register 220 to obtain permission to write to one of the temporary registers 210-222 corresponding to a desired timeslot. (*See*, col. 5, lines 56-60.) Applicants respectfully submit that the timeslot registers 210-220 corresponding to the various timeslots provided by AC '97 link do not disclose a register file, as recited by amended Claims 11 and 21.

Furthermore, the combination of Lewis in view of Potts fails to disclose either the selection units or control units, as recited by amended Claims 11 and 21, where the control unit directs a selection unit to activate a selected hardware accelerator to grant a processing element ownership of the selected hardware accelerator. Consequently, Applicants respectfully submit that the combination of Lewis in view of Potts fails to teach or suggest each recited feature of amended Claims 11 and 21, as required to establish a *prima facie* case of anticipation. In re Royka, supra.

Accordingly, amended Claims 11 and 21, for at least the reasons provided above, are patentable over the combination of Lewis in view of Potts. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11 and 21.

Regarding Claims 12-20 and 22-28, Claims 12-20 and 22-28, based on their dependency from Claims 11 and 21, respectively, are also patentable over the combination of Lewis in view of Potts. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 12-20 and 22-28.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-28 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 16, 2006

Marilyn Bass March 16, 2006